REMARKS

Claims 1, 2, 4, 6-14, 26-29, and 31, as amended, and new claims 33-35 appear in this application for the Examiner's review and consideration.

In particular, claim 1 has been amended to recite that the cap layer comprises diamond-like carbon (DLC), a feature that previously appeared in claims 30 and 32. Claims 10, 11, 14 and 27 have been amended for clarity. Claims 30 and 32 have been cancelled. New claims 33 to 35 are directed to preferred embodiments and are supported by paragraph [0037] of the published specification. The claim amendments and additions do not introduce new matter and for that reason should be entered at this time.

Claims 10-13, 14 and 27 were rejected under 35 USC section 112, second paragraph, for the reasons set forth on page 2 of the action. In response, claims 10, 11 14, and 27 have been amended to either provide explicit antecedent basis or to clarify the position of the sublayers. Thus, this rejection should be withdrawn.

Before addressing the prior art rejections, a brief review of the claimed invention may be helpful. The invention relates to forming a protective layer to the back side of a base wafer before transferring a layer on its top surface, preferably by a SMART-CUT® process. One application is to protect that surface from scratches that can occurs on a quartz base wafer when forming a silicon on quartz (SOQ) compound wafer. To do this, a cap layer of DLC is provided.

DLC is a very hard material such that a rather thin layer of this material can be used for forming an effective protection from mechanical damage (e.g., scratches) of the backside of, for example, a SOQ wafer. Obviously, forming a thin layer (20nm is the minimum thickness disclosed) offers the advantage of less material and less deposition time, and thus less cost.

In addition, there is a problem with deposition of relatively thick layers deposited on the backside of a quartz wafer when forming compound wafer by the SMART-CUT® process. The deposition of SiO2 and Si3N4 that can be found in the prior art may lead to impart stress to the material on which they are deposited. This stress is highly present for deposition of Si3N4 and may be present during deposition of SiO2 depending of the way the process is controlled. This is particularly true for thick layers that are needed to more efficiently protect against scratches (e.g., those more than about 1 micron for instance if protection is insured by SiO2). The stress that is formed due to deposition result in the quartz wafer presenting bows or warpage: the result is that the wafer is not perfectly flat.

The use of non-perfectly flat wafers in the SMART-CUT® process is very difficult, as this process comprises a bonding step that requires perfectly flat surfaces to insure good adhesion between the surfaces to be bonded. Therefore, the use of rather thick layers would not permit to form the SOQ wafer with sufficient quality according to the SMART-CUT® process. The use of a hard material like DLC provides sufficient hardness for avoiding scratches on the backside of the wafer, and also limits stress and deformations that are imparted to the quartz wafer because the required thickness is limited.

Claims 1, 2, 4-7, and 27-31 were rejected under 35 USC 102(b) as being anticipated by US patent 4.053,335 to Hu.

Hu discloses a method of gettering impurities away from devices formed at the surface of a silicon wafer. It includes the step of forming layers at the back side. The layer can include polycrystalline silicon and include additional layers of, for example, Si3N4. Hu does not disclose the steps recited in claim 1, namely, applying a top layer on a wafer and applying a cap layer comprising DLC to protect the back surface from damage. Thus, the anticipation rejection has been overcome and should be withdrawn.

Claims 1, 2, 5, 7, 8, 10, 12, and 27-31 were rejected under 35 USC 102(b) as being anticipated by US patent 4,687,682 to Koze, while claims 1, 2, 4-7, 9, 10, 12, and 26-32 were rejected under 35 USC 102(b) as anticipated by French patent application 2,454,697 to Thomson.

Both Koze and Thomson disclose methods of sealing the backside of a wafer before epitaxially growing a layer on the front side. The backside layers of Si02 and Si3N4 prevent diffusion of dopant from the backside to the front side of the wafer. Both Koze and Thomson do not disclose the steps of claims 1, namely, applying a cap layer comprising DLC to protect the back surface from damage. Thus, these rejections should also be withdrawn.

Claims 1, 2, 4-5, 7-8, 10-14, and 26-32 were rejected under 35 USC 102(b) as being anticipated by US patent 5,599,722 to Sakakibara.

Sakakibara discloses the step of forming an SOI wafer that includes steps of bonding an oxidized base wafer to a top wafer to form an SOI wafer. Although the oxidation is formed on both faces of the base wafer, this document does not disclose the use of a cap layer of DLC to protect the back surface of the base wafer from damage. Thus, the anticipation rejection has been overcome and should be withdrawn.

Claims 1, 2, 4-7, 9, 10, 12, and 26-32 were rejected under 35 USC 102(b) as being anticipated by European patent application 531,018 to SEH.

This document discloses the step of forming an SOI wafer, that includes steps of deposition of flattened polycrystalline layers and oxide on a top wafer (101), bonding the top wafer to a base wafer (111) and grinding the top wafer to form a SOI wafer. In this document, the deposition steps are formed on the top wafer, and no protective layer is formed on the base wafer. Thus, the anticipation rejection has been overcome and should be withdrawn.

Claims 1, 2, 4-7, 9, 10, 12 and 26-32 were rejected under 35 USC 102(b) as being anticipated by US patent 3,787,710 to Cunningham.

Cunningham discloses a method of forming a SOI wafer that includes forming an oxide layer on both sides of a top wafer; depositing a polycrystalline or amorphous thick layer on one face of the top wafer to form a base wafer and reducing the thickness of the top wafer to finally form an SOI wafer. Again, in this document there is no protection of the base wafer, which in this case is formed by deposition. Thus, this rejection should also be withdrawn.

As noted above, none of the references disclose the use of a cap layer of DLC to protect the back surface of a base wafer from scratches. Furthermore, the use of DLC provides unexpectedly better scratch resistance because DLC is a very hard material. In addition, only a rather thin layer of DLC material is needed for forming an effective protection from mechanical damage (e.g., scratches) of the backside of the wafer. And forming a thin layer offers the advantage of less material and less deposition time, and thus less cost. As none of these unexpected benefits are disclosed or taught by any of the cited references, it is respectfully submitted that the present claims are not obvious from any of the cited references.

In view of the above, it is believed that these claims are in condition for allowance, early notice of which would be appreciated. Should the examiner not agree, then a personal or telephonic interview is respectfully requested to discuss any remaining issues in an effort to expedite the eventual allowance of the application.

Respectfully submitted,

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